

EE143 – Fall 2016
Microfabrication Technologies

Lecture 11: Design Rules and Layout
Reading: Jaeger Chap. 9.2.2-9.2.4

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Design Rules

- **Interface between designer and process engineer**
- **Guidelines for constructing process masks**
- **Unit dimension: Minimum line width**
 - Scalable design rules: lambda parameter
 - Absolute dimensions (micron rules)

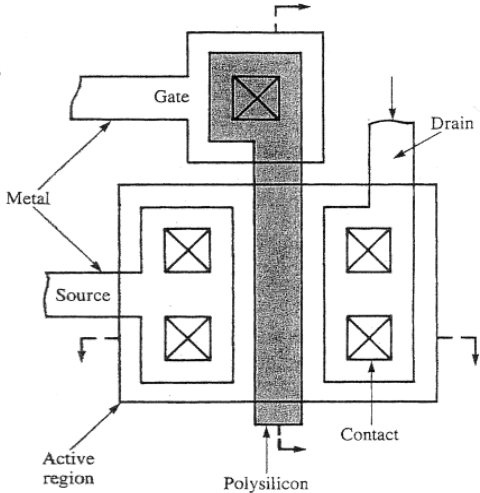


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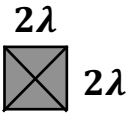
Layout Design Rules

- 1) Absolute-Value Design Rules
 - Use absolute distances
- 2) λ -based Design Rules

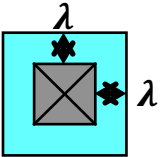


Metal-Si Contact Hole

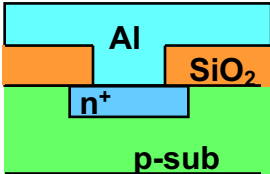
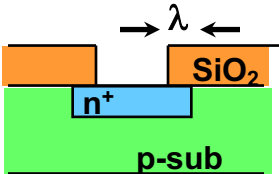
(same rule for Metal-poly)



Min. contact hole = $2\lambda \times 2\lambda$



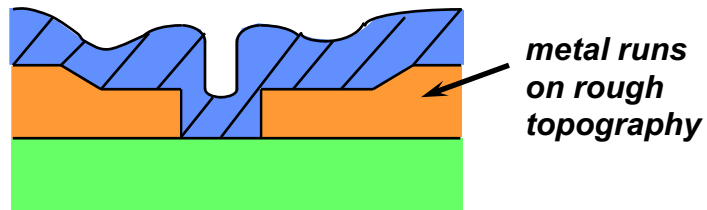
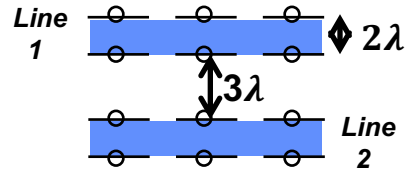
Min contact hole to diffusion layer distance = λ



Metal Lines

Min width = 2λ

Min. metal-metal spacing = 3λ



3λ spacing to ensure no shorting between the 2 lines

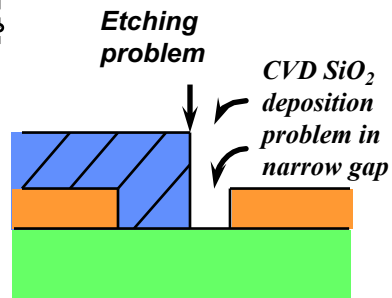
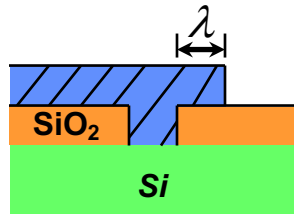
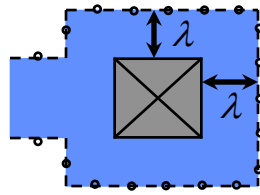


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M1-Contact Overlap

Min overlap of contact hole = λ

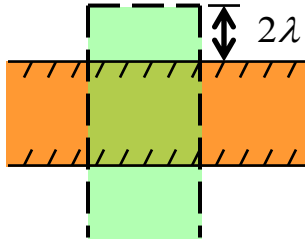


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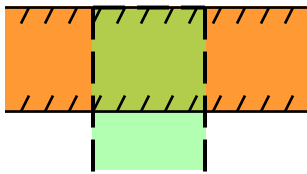


Poly-Si Gate

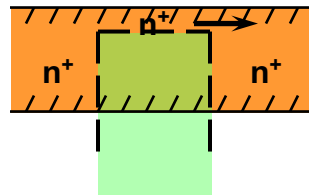
Min gate-overlap of field oxide = 2λ



Avoid n+ channel formation during S/D Implant



Ideal



With overlay error

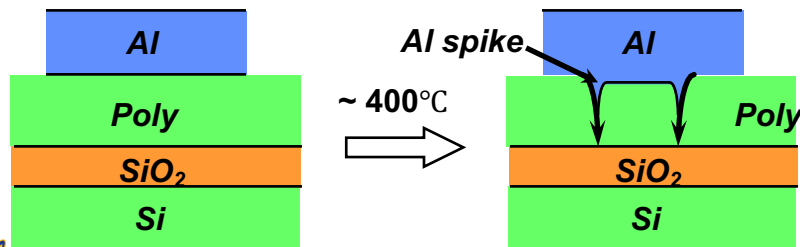
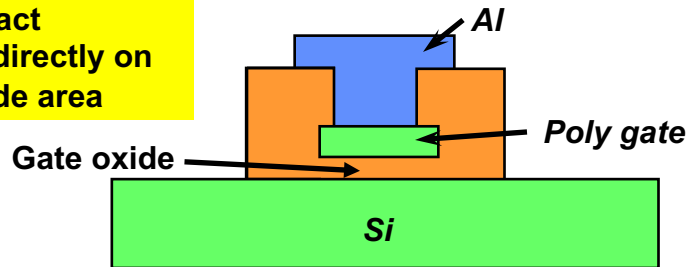


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Gate Contacting

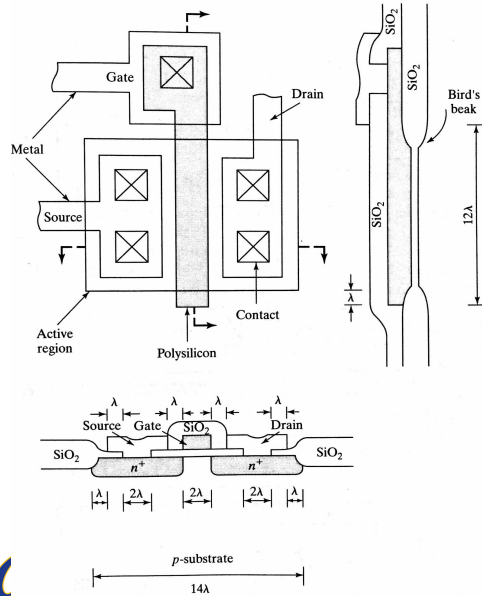
Comment:
Al to poly contact
should not be directly on
top of gate oxide area



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Layout of Polysilicon Gate MOSFET

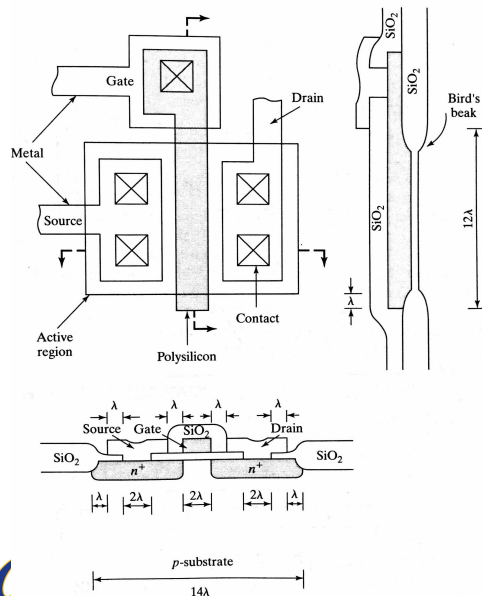


4 mask process:

- 1) Active region (thin oxide) mask
- 2) Polysilicon mask
→ Aligned to level 1
- 3) Contact window mask
→ Aligned to level 2
- 4) Metal mask
→ Aligned to level 3



Layout of Polysilicon Gate MOSFET



- Example for poly-Si MOSFET with $W/L = 5$
 - L: channel length
 - W: channel width
- Minimum width in X direction = 14λ
- Minimum width in Y direction = 12λ (not counting the Al-poly contact)
- Transistor area = $14\lambda \times 12\lambda = 168\lambda^2$
- Active channel area = $20\lambda^2$ (12% of transistor area)

